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Design of an ASIC Digital Clock Using VLSI Technology

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Abstract: We present the design of an Application Specific Integrated Circuit (ASIC) digital clock based on the 0.12 μm deep submicron technology node. The widths of the PMOS and NMOS transistors are 0.72 μm and 0.24 μm, respectively. The clock expresses time based on the 12-hour time notation. The gate-level schematic and the layout of the design are drawn and validated using DSCH3 and Microwind3 Lite. The key feature of the clock is constructed from 18 D-type flip-flops. Two modulo-60 counters and a modulo-12 counter are built from the flip-flops. The modulo-60 counters are used for the second and minute modules, while the modulo-12 flip-flop is for the hour module. The length and width of the layout are, respectively, 153.60 μm and 58.14 μm. This is to say that the size of the die is comparable with that of a human hair. The average static power dissipation is found to be 0.202 mW, which is reasonably low. Since the proposed design is in the form of an ASIC chip, the input and output pins merely require to be connected to an external power source, an oscillator, and displays, to allow the clock to operate properly. With its miniaturized size and low power consumption, the proposed design clearly exhibits advantages over those built using discrete components and general-purpose chips.

Keywords: ASIC; Deep submicron technology; Digital clock; Modulus counter; VLSI.

1. INTRODUCTION

The first digital clock built using the liquid crystal display technology could be dated back to the 1960s [1]. Since the process of construction was laborious and that the amount produced was scarce then, the prices of these clocks were relatively expensive. The Hamilton pulsar released in 1972, for instance, cost $ 2,100 – which was about the price of a small car at that time [1]. Within the span of less than 50 years, however, a digital clock could now be easily acquired with the price below $ 5. The dramatic reduction in the price of digital devices in general, and digital clocks in particular, is essentially due to the rapid technology advancement in microchip fabrications [2 – 4]. Unlike in the old days where a digital device was built based on the integration of multiple discrete components; a device with identical functions today may rely solely on one microchip – such as a microcontroller. The implementation of a single microchip not only curtails the number of components deemed necessary to build the devices, it also simplifies the complexity of the construction process.

A search in the literature reveals that most digital clocks nowadays are widely designed and built using general-purpose chips such as microcontrollers [5 – 8] and Field Programmable Gate Arrays (FPGAs) [9 – 12]; while some are still based on discrete components [13, 14]. To the best of the authors' knowledge, designs and discussions based on the employment of Application Specific Integrated Circuits – or more colloquially referred to as ASICs – are not available in the literature. Since an ASIC tends to optimize the number of components used and the size of the chip, it clearly exhibits advantages over those using the other methods.

In this paper, we present a detailed explanation on the design of a digital clock and its corresponding layout used for a Very-Large-Scale-Integration (VLSI) ASIC. In our study, we shall consider the size, the number of transistors involved, and the static power dissipation of the chip. As shall be demonstrated in the subsequent sections, the layout only constitutes an approximate area of 8.93×10^{-9} m^2 when the 0.12 μm deep submicron technology node is used, with 507 transistors involved in the circuit. The average static power dissipation is also found to be as low as 0.202 mW. Since the chip is designed specifically for a digital clock, i.e., it is an ASIC-based VLSI clock, its size is clearly much smaller and power consumption much lower compared to a clock built using either general-purpose chips or discrete components.

2. CIRCUIT DESIGN

The proposed digital clock comprises the hour, minute, and second modules which are constructed from modulo-60 (MOD-60) and modulo-12 (MOD-12) counters. The main components used to construct the counters are D-type flip-flops (DFF) and combinational logic gates.

The D-type flip-flop is the fundamental building block for the counters, and it consists of four input pins – the data input (*D*), reset (*RST*), and clock (*CLK*) pins and two output pins – the output Q and inverted output $\bar{Q}$ pins, as shown in Figure 1. Since an active-low flip-flop is employed, the output will be toggled (i.e. it will change from logic one to zero and vice-versa) every time the clock goes low. The Q pins of the flip-flops denote the binary coded decimal or BCD codes and are to be connected to the seven segments displays.

Since the minute and second modules count from 0 to 59, their circuit designs are rather similar. In this sense, seven DFFs are used to construct the modulo-60 (MOD-60) counter for these two modules – three of which form a modulo-6 (MOD-6) counter which is catered for the tens place and the remaining form a modulo-10 (MOD-10) counter for the ones place. As can be seen from the gate-level schematic of the second module in Figure 2, the outputs of flip-flops *D*0 and *D*3 represent the least significant bits (LSBs); while the outputs of *D*2 and *D*6 represent the most significant bits (MSBs) of the tens and ones places, respectively. Likewise, the LSBs and MSBs for the tens and ones places of the minute module in Figure 3 are given by the outputs of the leftmost (i.e., *D*7 and *D*10) and rightmost flip-flops (i.e., *D*9 and *D*13), respectively. It can be seen from both figures that, the outputs of flip-flops *D*4 and *D*6 of the second module and flip-flops *D*11 and *D*13 of the minute module are connected separately to a 2-input AND gate. When the ones place exceeds 9, the output pins of *D*4, *D*6, *D*11, and *D*13, which are connected to the AND gates, produce a logic one. The AND gates then trigger the *RST* pins of *D*3 and *D*10, thereby resetting the LSBs. This is to say that flip-flops *D*3 to *D*6 of the second module and *D*10 to *D*13 of the minute module form a MOD-10 counter which iteratively counts from 0 to 9.

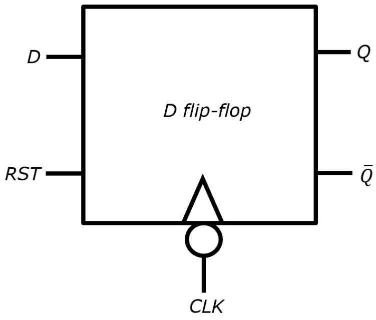


Figure 1. A D-type flip-flop

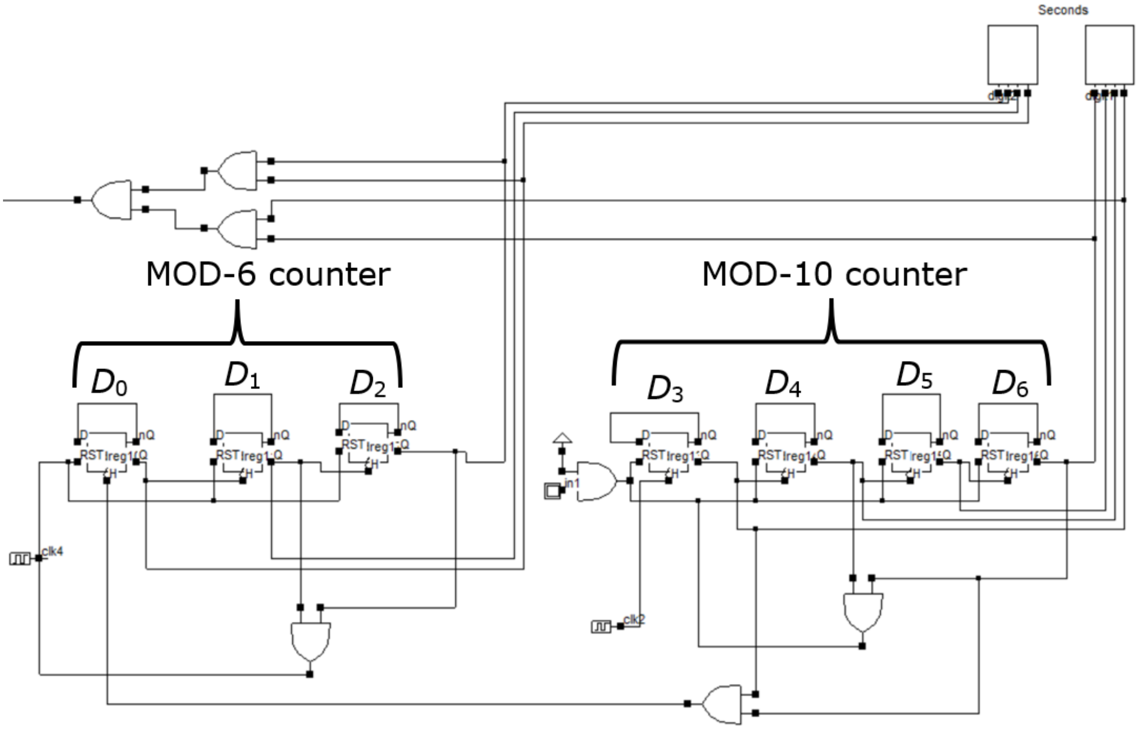


Figure 2. The gate-level schematic of the second module

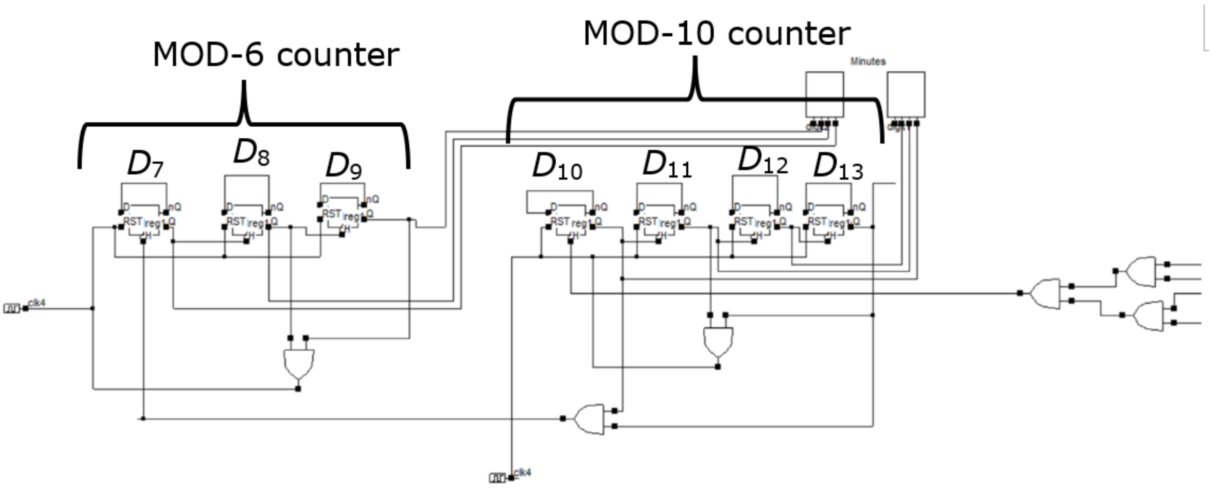


Figure 3. The gate-level schematic of the minute module

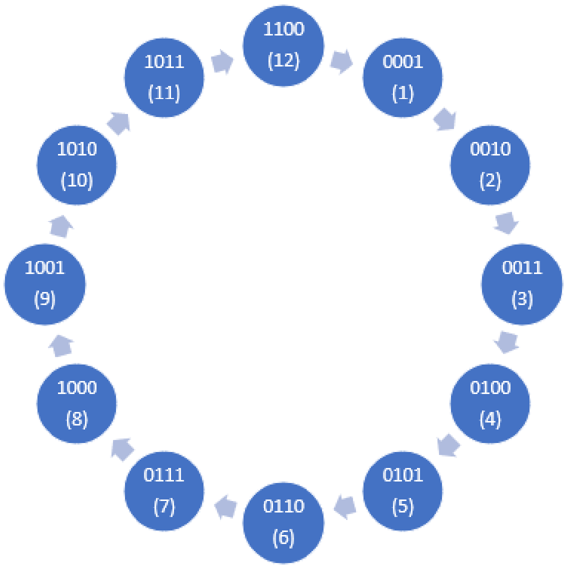


Figure 4. State graph for the MOD-12 counter

Figures 2 and 3 also show that the outputs of $D4$, $D6$, $D11$, and $D13$ are connected to the clock pins of the tens place, via AND gates. This is to increment the tens place every time the output pins at the ones place exceed 9. Like the case of the ones place, the outputs of $D1$ and $D2$ of the second module and $D8$ and $D9$ of the minute module are connected separately to an AND gate. Each time these flip-flops transmit a logic one to the gate, outputs at $D0$ and $D7$ will be reset. Hence, the first three counters from the left of Figures 2 and 3 act as a MOD-6 counter which iteratively counts from 0 to 5. By combining both MOD-6 and MOD-10 counters, a MOD-60 counter which counts from 0 to 59 is then materialized. It is worthwhile noting that when the second module counts 59, the LSBs and MSBs give logic ones simultaneously. In order to activate the minute module at the next clock pulse after the second module counts 59, these four pins are therefore fed to two AND gates. As shown in Figures 2 and 3, the two AND gates are connected using a third AND gate and the output of which triggers the *CLK* pin of $D10$.

Designing the hour module is, perhaps, the most challenging part of the ASIC clock. This is because a typical modulus counter starts its count from zero. This condition is invalid for the hour module since it always counts from one for each cycle. In order to circumvent the count of zero, we have constructed a state graph for the MOD-12 counter, as shown in Figure 4 and tabulated a state table based on it. As can be seen in Table 1, DFFs $D14$ to $D17$ have been used to generate the four digits binary outputs which counts from 1 to 12 or 0000 to 1100 in binary format. By simplifying the state table using Karnaugh maps, the following relationships for the DFFs are obtained

$$D_{D14} = Q_{D15}Q_{D16}Q_{D17} + Q_{D14}\overline{Q_{D15}} \tag{1}$$

$$D_{D15} = \overline{Q_{D14}}Q_{D15}(\overline{Q_{D16}} + \overline{Q_{D17}}) + \overline{Q_{D15}}Q_{D16}Q_{D17} \tag{2}$$

Table 1. State table for the hour module

Q_{D14}	Q_{D15}	Q_{D16}	Q_{D17}	Q_{D14}^{+}	Q_{D15}^{+}	Q_{D16}^{+}	Q_{D17}^{+}	D_{D14}	D_{D15}	D_{D16}	D_{D17}
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	0	0	0	1	0	0	0	1

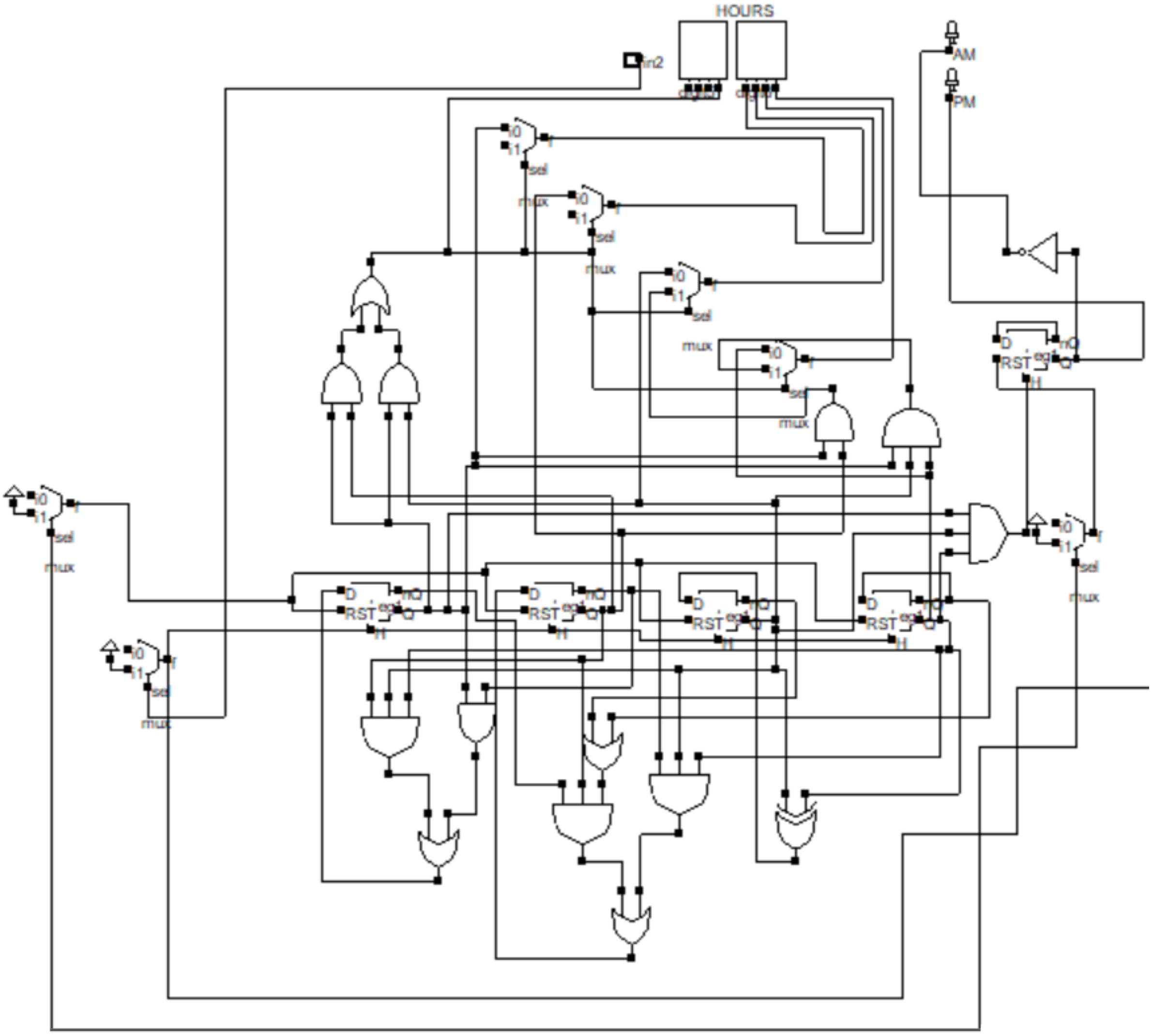


Figure 5. The gate-level schematic of the hour module

$$D_{D16} = Q_{D16} \oplus Q_{D17} \tag{3}$$

$$D_{D17} = \overline{Q_{D17}} \tag{4}$$

where *D* and *Q* are, respectively the input and output of the flip-flop and the subscript denotes the flip-flops. The gate-level schematic for the hour module, constructed based on (1) to (4) is shown in Figure 5.

Figure 6 depicts the full logic gate-level schematic of the digital clock design. As can be observed from the figure, the clock integrates the hour, minute, and second modules. It can also be seen that switches and seven-segment displays are used in the design, so that the values of the modules can be adjusted and shown. It is to be noted that 2-to-1 multiplexers have been introduced into the circuit so as to let the user to adjust the time. When the input of the selector switch is fed with a logic zero, the clock tends to count its time by itself; when input is logic one, however, the count pauses and the user is then allowed to adjust the value of each module. Besides switching between these two modes, the multiplexers also act as current buffers for the DFFs.

3. RESULTS AND DISCUSSION

The operation of the schematic in Figure 6 is validated using the DSCH3 simulator. The 0.12 µm deep submicron technology file is selected, with the widths of the PMOS and NMOS transistors are given as 0.72 µm and 0.24 µm, respectively. The circuit is switched on and left to run for two cycles – from time 00:00:00 am to 12:00:00 pm and then back to 00:00:00 am again. Figures 7 to 10 summarize the values shown at the seven-segment displays at various critical time conditions and their corresponding timing diagrams. Figure 7 depicts the initial condition when the clock is activated, with all its modules reset to zero (i.e., at 00:00:00 am). As clearly illustrated in Figure 8, the second module resets to zero and the minute module increments by 1 at the next clock pulse after the second module counts 59 (i.e., from 00:00:59 am to 00:01:00 am). As mentioned in the preceding section, both the circuit designs of the second and minute modules are rather similar. Hence, like the case of its second counterpart, the minute module resets back to zero and, at the same time, the hour module increments by one at the next clock pulse when the time is at 59 minutes, as depicted in Figure 9 (i.e., from 00:59:59 am to 01:00:00 pm). It can also be observed from Figure 10 that the clock operates accurately during its transition from 12:59:49 pm to 01:00:00 am.

To generate the physical layout of the design, the architecture of the clock is exported to the Microwind3 Lite software. Figure 11 depicts the final layout of the clock once the floor planning, placement, and routing processes are completed. The layout has been verified by the Design Rule Checker (DRC) to ensure that it complies with the manufacturing requirements. Upon inspection, the layout is found to constitute a total of 273 NMOS and 234 PMOS transistors, with a size of approximately 58.14 µm × 153.60 µm. This size is comparable to the average diameter of flaxen (50 µm) and black hair (181 µm) [15]. The average static power dissipation is found to be 0.202 mW, which is reasonably low.

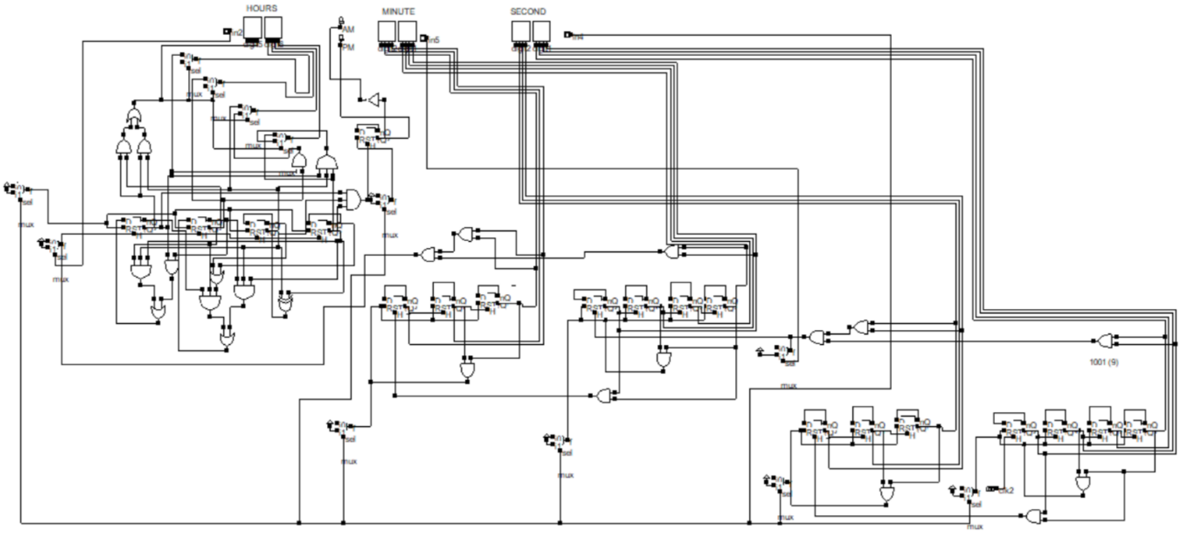


Figure 6. Complete gate-level schematic of the digital clock

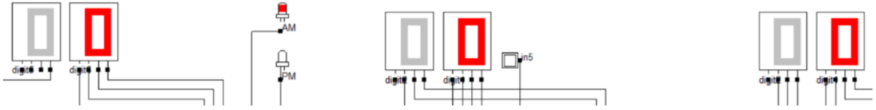
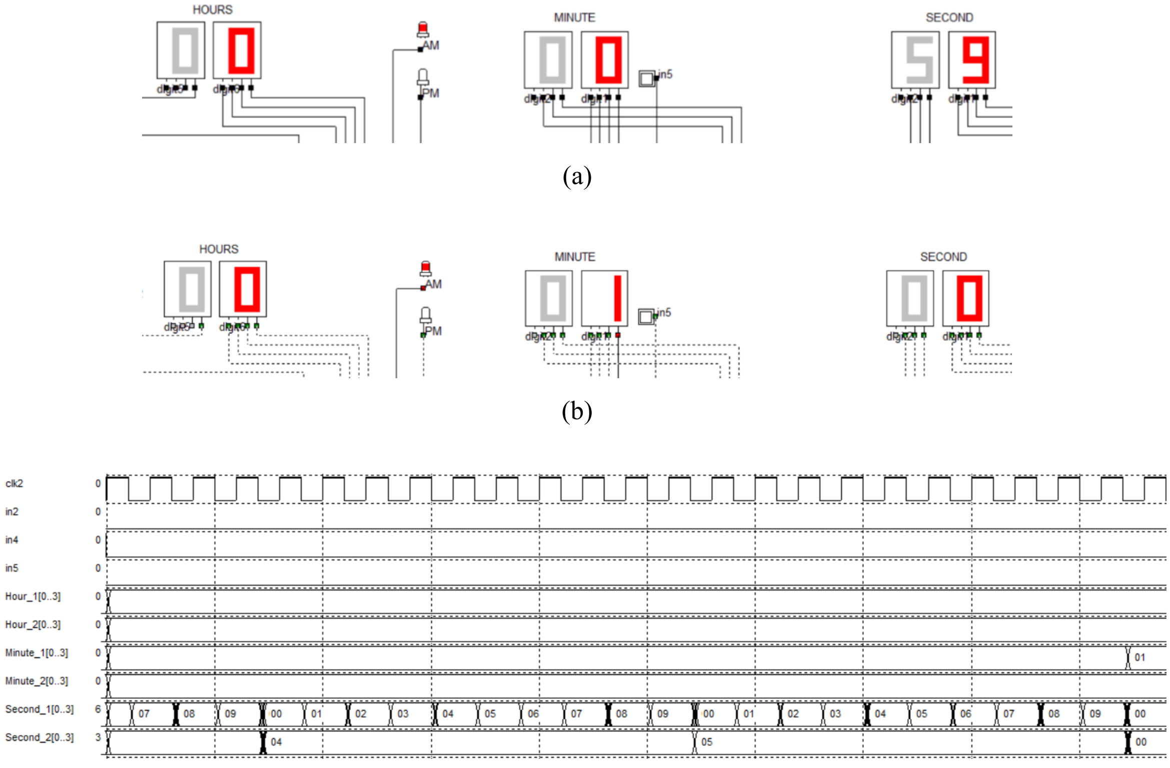


Figure 7. At the initial condition, the time is reset to 00:00:00 am

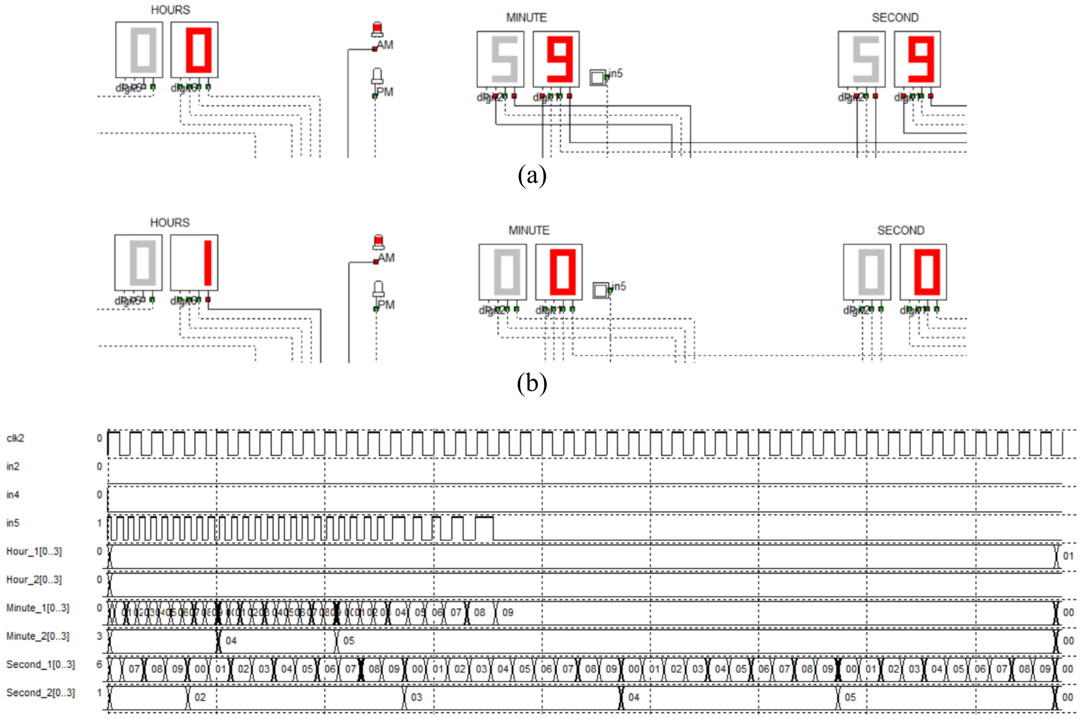


(a)

(b)

(c)

Figure 8. The transition of time from (a) 00:00:59 am to (b) 00:01:00 am after the next clock pulse and (c) its corresponding timing diagram

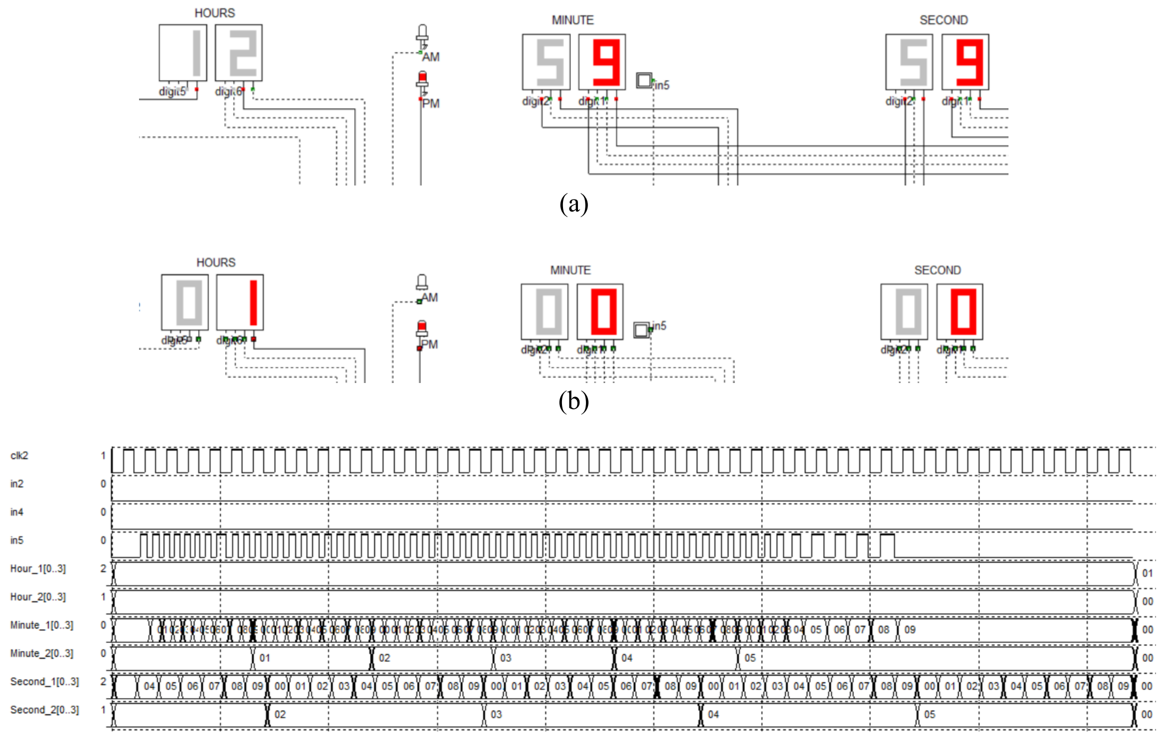


(a)

(b)

(c)

Figure 9. The transition of time from (a) 00:59:59 am to (b) 01:00:00 am after the next clock pulse and (c) its corresponding timing diagram



(a)

(b)

(c)

Figure 10. The transition of time from (a) 12:59:59 pm to (b) 01:00:00 pm after the next clock pulse and (c) its corresponding timing diagram

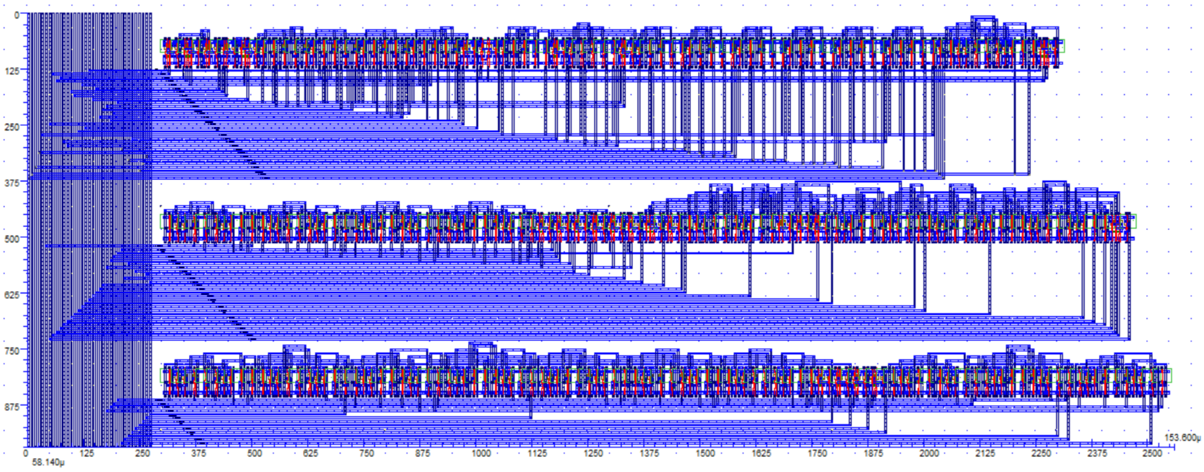


Figure 11. The physical layout of the proposed digital clock

4. CONCLUSION

In this paper, the design of an ASIC digital clock based on the 12-hour notation is proposed. The clock is constructed from D-type flip-flops, combinational logic gates, and multiplexers. The 0.12 µm technology file is used, when generating the physical layout of the clock, with the widths of the PMOS and NMOS transistors are given respectively as 0.72 µm and 0.24 µm. The circuit and layout representations have been validated using DSCH3 and DRC in Microwind3 Lite. The size of the layout is approximately 58.14 µm × 153.60 µm which is analogous to the average diameter of a human hair. The average static power dissipation of the chip constitutes 0.202 mW, which is reasonably low. A functional clock can be easily constructed from the chip by connecting its input and output pins to an external power source, an oscillator, and displays. With its miniaturized size and low power consumption, the proposed design clearly exhibits advantages over those built using discrete components and general-purpose chips.

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