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Benchmarking Study of Ballistic Current Transport Equations in Symmetric Double-Gate nano-MOSFET by Using Numerical Calculations and Simulation

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Abstract: Five electron transport models for drain current equations of symmetric 10 nm Silicon-based (Si-based) double-gate (DG) nano-MOSFET have been numerically investigated in this paper. All these models are based on ballistic transport flow. The first model, named full ballistic model, assumed no backscattering to the source and produced an on-state drain current of 1.137×10^3 µA/µm. The second model, named electrostatic model which based on electrostatic, included scattering and produced on-state drain current of 2.182×10^3 µA/µm. Whereas the third model, named flux-theory model, and fourth model, named flux-theory corrected model, were analyzed using flux-theory concept of electron flow and then two different drain current equations were obtained. However, both models producing almost the same value of on-state drain current 2.548×10^3 µA/µm numerically. Finally, the fifth model, named space charge model, utilized the concept of subband and electron charge distribution on k-space, producing on-state current of 2.241×10^3 µA/µm. All these models treat electron flow quantum mechanically. Thus, all five computed on-state currents were benchmarked against an on-state current simulated using online device simulator nanoMOS which outputted Si-based ultra-thin channel nano-MOSFET norminal on-state drain current of 2.500×10^3 µA/µm. The flux-theory models are found to be the most compatible to simulation result because flux-theory model can be generalized for multi-subband, various materials and arbitrary wafer orientations. On the other hand, the first model without backscattering consideration exhibited the least accurate result due to the fact that scattering cannot be ignored in formulating quantum ballistic transport models. The accuracy of this benchmarking evaluation showed that highly sophisticated electron transport numerical models must incorporated ballistic quantum nature effects as well as scattering effects when developing commercial device simulation tools such as TCAD.

Keywords: Current equation; Electron transport; Nano-MOSFET; Quantum effects; Scattering.

1. INTRODUCTION

Si-based integrated circuits (ICs) have dramatically shrinking in size due to rapid downscaling of MOSFET channel length to nanometer regime [1-3]. However, the continuous downscaling of channel length leads to deterioration of device performance because of the short channel effects (SCEs) [4-6]. In order to eliminate this weakness, multiple-gate MOSFET structure, such as double-gate (DG), gate-all-around (GAA) and quadruple-gate, have been proposed and being investigated as the promising candidates to replace classical bulk MOSFETs for utilization in modern consumer electronic products [7-9]. The main challenge faced during this process is that device scientists need to reexamine and replace traditional classical physic-based electron transport models with quantum mechanical oriented electron transport models. Unfortunately, study of these quantum models requires sophisticated computing power in order to carry out complex numerical computations [10-12]. Therefore, the objective of this paper is to study a few drain current compact models of Si-based symmetric DG nano-MOSFET with online device simulator tool nanoMOS [13-14]. This will facilitate and help device engineers to better exploit DG nano-MOSFET in logic circuits design and simulation [15-16]. In this paper, theories of drain current models of 10 nm DG nano-MOSFET have been incorporated computationally into open-source online device simulator [17].

2. DEVICE DESIGN

The symmetric DG nano-MOSFET device structure which is used in this nanoMOS benchmarking simulation project is shown in Figure 1 [18].

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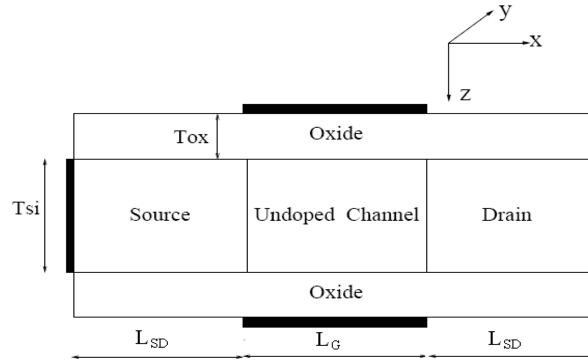

Figure 1. Double-gate nano-MOSFET device structure diagram

Table 1. Double-gate nano-MOSFET device structural parameters

Simulation Parameters Setting of Double Gate nano-MOSFET			
Drain-to-source voltage bias (V_{DS})	0.60 V	Channel length (L)	10 nm
Gate-to-source voltage bias (V_{GS})	0.60 V	Top/bottom oxide insulator thickness (T_{OX})	1.5 nm
Threshold voltage (V_T)	0.20 V	Top/bottom insulator relative dielectric constant	3.9
Ambient temperature	300 K	Longitudinal relative electron mass ratio (m_l)	0.98
Source/drain doping concentration (N_D)	$1x10^{20}$ cm^{-3}	Transverse relative electron mass ratio (m_t)	0.19
Body doping concentration	0 cm^{-3}	Channel body relative dielectric constant	11.7
Silicon channel thickness (T_{Si})	1.5 nm	Top/bottom gate contact work function	4.188 eV
Source/drain overlap	0 nm	Silicon conduction band valleys	unprimed
Source length/drain length (L_{SD})	7.5 nm	Number of subbands	1

The channel material used is Silicon. Silicon is the most commonly used semiconductor material nowadays due to its mature fabrication technology and also the fact that Si is one of the most abundant materials on the earth. Thus, eliminating any worries about availability. The device structural simulation parameter settings are listed in Table 1. The conduction band valleys chosen is unprimed subbands and the total number of subbands is set to 1. Wafer orientation is (001) with translational direction [100].

The device parameters in Table 1 are chosen such that the electrons in the channel of the DG nano-MOSFET have quantum mechanical properties in nature instead of possessing particle nature property as in classical bulk MOSFETs. Therefore, the device structural dimension should be on the order of atomic scale (Si lattice). In other words, the structural parameters should be in nanometer regime [18].

3. REVIEW OF CARRIER TRANSPORT MODELS

The first transport model, named full ballistic model, which is investigated in this paper is based on assumption that electrons do not encounter scattering when injected into the channel or in other words without backscattered to the source reservoir [19-20]. The ballistic drain current per micron width is as

$$\frac{I_D}{W} = Q_0 v_\theta \tag{1}$$

where $v_\theta = \sqrt{2k_B T/\pi m_t^*}$ is the ballistic velocity of electron which is thermal velocity v_T in the non-degenerate limit. $m_t^*$is the transverse effective mass. Q_0 is the top of potential barrier inversion charge which is independent of the scattering in the channel. In saturation region, $Q_0 = C_{ox}(V_{GS} - V_T)$ for DG nano-MOSFET where $C_{ox} = (3.9 \times \varepsilon_o \times 2)/T_{ox}$ is the gate oxide capacitance per unit area for DG nano-MOSFET. $V_{GS}, V_T, \varepsilon_o$ and T_{ox} are the gate-to-source voltage, he threshold voltage, the permittivity of free space and the oxide insulator thickness.

The second drain current model (also named electrostatic model) is based on electrostatics including backscattering as described in [19]. Figure 2 shows this phenomenon [20]. The expression for drain current per micron width is

$$\frac{I_D}{W} = BC_{ox}v_T(V_{GS} - V_T)\left[\frac{1-\frac{\mathcal{F}_{1/2}\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_{1/2}(\eta_{F1})}}{1+\frac{\mathcal{F}_0\left(\eta_{F1}-\frac{qV_D}{k_BT}\right)}{\mathcal{F}_0(\eta_{F1})}}\right] \tag{2}$$

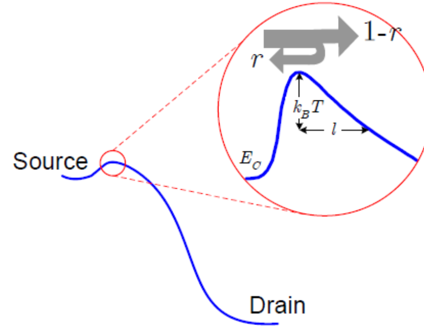

Figure 2. Backscattering coefficient *r*, critical length *l* and thermal voltage k_BT/q labelled at potential barrier

where B is the ballistic efficiency, $\mathcal{F}_j$ is the Fermi-Dirac integral of order *j* and $\eta_{F1} = (\epsilon - E_i)/k_BT$ with E_i is the energy level taken at region around top of the barrier and ϵ is the average energy level between source and drain. v_T is the thermal velocity, V_D is the drain voltage, k_B is the Boltzmann constant and T is the ambient temperature.

The third (also named flux-theory model) and fourth (also named flux-theory corrected model) electron transport models are based on flux-theory approach [21]. Two assumptions have been proposed. Firstly, in equilibrium conditions, source and drain are considered ideal reservoirs of electrons. Secondly, SCEs are neglected due to perfect gate control over the potential barrier. The flux $F_s{}^+$, which is emitted from source reservoir in equilibrium, is given by

$$F_s{}^+ = \frac{(2kT)^{3/2}}{\pi^2\hbar^2}\left[\sum_i \sqrt{m_{cL}} F_{1/2}\left(\frac{E_{Fs}-E_i{}^L}{k_BT}\right) + \sum_i \sqrt{m_{cT}} F_{1/2}\left(\frac{E_{Fs}-E_i{}^T}{k_BT}\right)\right] \quad (3)$$

where $m_{cL} = m_t$, $m_{cT} = \left(m_l{}^{1/2} + m_t{}^{1/2}\right)^2$, $F_{1/2}$ is the Fermi-Dirac integral of order 1/2, *i* the subband index, $E_i{}^L$ is unprimed subband energies, E_{Fs} is the source Fermi level and $E_i{}^T$ is primed subband energies. Meanwhile, the flux $F_d{}^-$ emitted from drain is expressed as

$$F_d{}^- = \frac{(2kT)^{3/2}}{\pi^2\hbar^2}\left[\sum_i \sqrt{m_{cL}} F_{1/2}\left(\frac{E_{Fd}-E_i{}^L}{k_BT}\right) + \sum_i \sqrt{m_{cT}} F_{1/2}\left(\frac{E_{Fd}-E_i{}^T}{k_BT}\right)\right] \quad (4)$$

with the drain Fermi level, $E_{Fd} = E_{Fs} - qV_{DS}$, Equation (4) becomes

$$F_d{}^- = \frac{(2kT)^{3/2}}{\pi^2\hbar^2}\left[\sum_i \sqrt{m_{cL}} F_{1/2}\left(\frac{E_{Fs}-qV_{DS}-E_i{}^L}{k_BT}\right) + \sum_i \sqrt{m_{cT}} F_{1/2}\left(\frac{E_{Fs}-qV_{DS}-E_i{}^T}{k_BT}\right)\right] \quad (5)$$

where $\hbar$ is the reduced Planck's constant and V_{DS} is the drain-to-source voltage. The unit of flux is per cm sec [22]. These two equations can be generalized for the case of multi-subbands, various materials and arbitrary wafer orientation. The unprimed subbands have lower bound-state energies than primed subband because of heavier longitudinal mass causing them primarily populated by electrons. Therefore, it is sufficient to consider only one conduction band unprimed subband. By using Equations (3) and (5), the first ballistic drain current per micron width flowing from source to drain is expresses as

$$\frac{I_d^{BAL}}{W} = q(F_s{}^+ - F_d{}^-) \quad (6)$$

where q is the elementary electronic charge. Further assumption states that at high field situation, the drain terminal is unable to emit electrons which is capable of reaching the source. By applying flux-theory method, this leads to second drain current expression as

$$\frac{I_d^{BAL}}{W} \sim qF_s{}^+ \quad (7)$$

In next section on discussion, it is reported that these two equations yielded almost the same result.

The fifth model (also named space charge model) is based on quantization of energy levels in nanostructure [19]. Quantization produces many energy levels and so multi-subbands. The distribution of charges in *k*-space at the potential barrier is symmetric in equilibrium state and hence resulting in zero net current. However, in off-equilibrium state, the charges distribution is asymmetric in *k*-space. In ballistic regime, +*k* states are inhabited according to the source Fermi level. Meanwhile, -*k* states are populated according to drain Fermi level. This situation is shown in Figure 3. The black circles in Figure 3 represent the space states that are occupied by electrons.

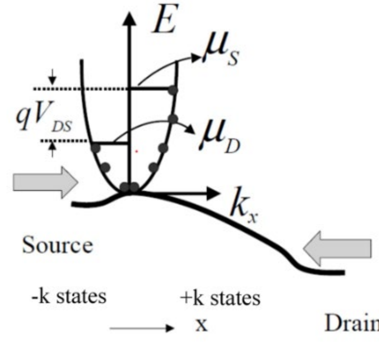

Figure 3. A schematic diagram showing distribution of charges in k-space at non-equilibrium condition

The difference in Fermi levels between source and drain is qV_{DS}. The total charge is still the equilibrium charge but the distribution is not equilibrium distribution. This difference in population between the k states results in a net drain current as can be evaluated by using the formula as

$$\frac{I_{Di}}{W} = I_{0i}\{F_{1/2}[(\mu - E_i)/k_BT] - F_{1/2}[(\mu - E_i - qV_{DS})/k_BT]\} \tag{8}$$

where $F_{1/2}$ is the Fermi-Dirac integral of order ½ and I_{0i} is a coefficient for subband i, as state in Equation (9) with dimension of current per unit length. In this paper, consider only conduction band unprimed valley with one subband due to reason stated above.

$$I_{0i} = \frac{q}{\hbar^2}\sqrt{\frac{m_C}{2}}\left(\frac{k_BT}{\pi}\right)^{3/2} \tag{9}$$

where $m_C = 4m_t$.

4. RESULTS AND DISCUSSION

The drain current versus drain-to-source voltage bias (I-V curve) and subband energy profile along the channel simulation output plots of nanoMOS are shown in Figures 4 and 5, respectively. Since the 10 nm DG nano-MOSFET is aimed for designing logic gates, voltage biasing 0.60 V is chosen because it is the on-state saturation operating point for transistor level logic circuits [23-24]. From Figure 4, the simulated on-state drain current norminal value is 2.500 x10^3 µA/µm which is used as a benchmarking candidate for drain current calculation results of the five models presented in Section 3. This benchmarking data is obtained by simulating quantum properties as listed in Table 1 with nanoMOS by solving Schrodinger Equation with Non-Equilibrium Green's Function (NEGF) formalism coupled with Poisson Equation. The subband energy profile in Figure 5 is needed for Fermi integrals calculations.

According to the first model, using equations for C_{ox} and v_θ, both parameters are computed to be equal to 4.604x10^{-2} F/m^2 and 1.234x10^5 m/s, respectively. So, inversion charge, Q_0 is equals to 9.208x10^{-3} C/m^2. Then, by using Equation (1), I_D/w is calculated numerically to be equal to 1.137x10^3 µA/µm, which is 45.48% of benchmarking value. The reason is that this model assumed ballistic flow without considering scattering back to the source due to subband energy profile. Actual physical electron transport models should include scattering mechanisms for accuracy. This drawback is overcome by including scattering in quantum transport model expressed in Equation (2), as shown diagrammatically in Figure 2. The subband energy profile in Figure 5 is used to evaluate the on-state drain current according to Equation (2) by taking energy levels at region around top of the barrier (-0.12 eV) at channel position -5 nm and between source and drain (-0.4 eV) which is the average energy between source (-0.1 eV) and drain (-0.7 eV), that is $\eta_{F1} = (\epsilon - E_i)/k_BT = ((-0.4 - (-0.12))/k_BT) \times q = -10.83$. Lastly, the computed value is 2.182 x10^3 µA/µm where the detailed calculation steps can be found in reference [25]. When compared with the benchmarking value, the percentage of matching is 87.28% which is obviously better than the first model since there will always have scatterings in real practical nanodevices [26-27].

The electrical characteristics of the 10 nm DG nano-MOSFET under studied are all quantum mechanically in nature and so the above two models are expected to be unable to fully described the ballistic transport in nanostructures. Therefore, third (see Equation (6)) and fourth (see Equation (7)) models based on flux-theory approach have been proposed. In ultra-thin Si body, which is 1.5 nm in this paper, the energy levels splitting due to quantization are significantly greater than thermal voltage and hence electrons are only can occupy the bottom subband. This prevents hopping to higher energy levels [28]. Thus, using only unprimed valley and one subband is sufficient for explaining the ballistic current flow. Using Figure 5, Equation (3) and Equation (5), F_s^+ is 1.590x10^{22} cm^{-1}s^{-1} and F_d^- is 8.239x10^{12} cm^{-1}s^{-1}, respectively.

The steps are as following:

a) Calculate F_s^+, $\frac{E_{Fs}-E_i{}^L}{kT} = \frac{source\ Fermi\ level - Fermi\ level\ at\ the\ device\ center}{kT} \times q = \frac{(-0.1258)-(-0.1700)}{kT} \times q = 1.709$

b) Calculate F_d^-, $\frac{E_{Fd}-E_i{}^L}{kT} = \frac{drain\ Fermi\ level - Fermi\ level\ at\ the\ device\ center}{kT} \times q = \frac{(-0.6784)-(-0.1700)}{kT} \times q = -19.670$

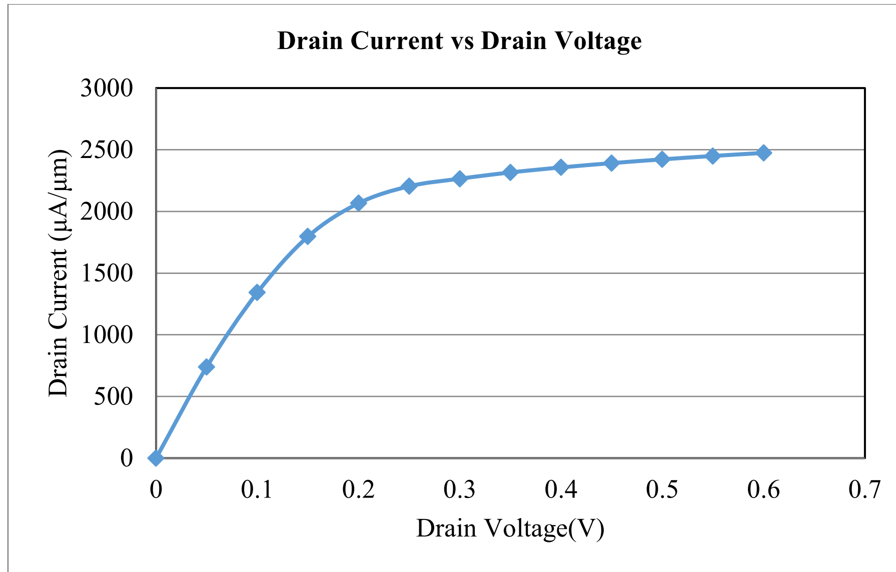

Figure 4. Drain current against drain-to-source voltage curve. The current value at drain voltage 0.6 V is the norminal on-state drain current of 2500 µA/µm

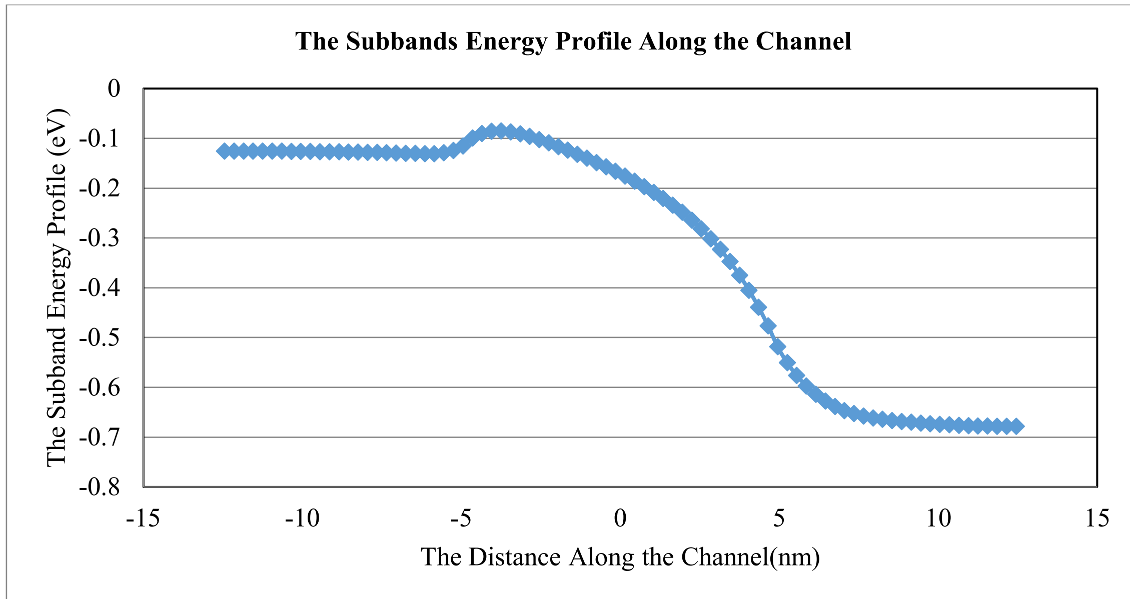

Figure 5. Subband energy profile along the channel

Hence, the ballistic drain current is 2.548x10^3 µA/µm as obtained from Equation (6). In high field conditions where the drain reservoir is no able to emit electrons capable of travelling to the source, I_d^{BAL}/w can be approximated to Equation (7) which has a value of 2.548x10^3 µA/µm which is very close to Equation (6) result. From this analysis step, it is evident that both flux-theory models are almost 100% matched the benchmarking value. Thus, flux-theory approach is the best way to describe the quantum ballistic transport in symmetric 10 nm DG nano-MOSFET, or in other words, ultra-short and ultra-thin nano-MOSFET [29-30].

Another way to evaluate the performance of quantum ballistic drain current is using charge distribution in *k*-space at potential barrier as stated in Figure 3 and Equation (8). For unprimed valley with single subband, I_{01} is 4.059x10^2 A/m according to Equation (9). After using Equation (8) and Figure 5 (energy levels values are the same as flux-theory model), the computed ballistic drain current is 2.241x10^3 µA/µm, which is 89.64% matched the benchmarking value. Thus, this fifth model has nearly the same efficiency as the second model in describing electron transport in semiconductor nanodevices. The comparison results are tabulated in Table 2.

Table 2. Drain current values comparison between different models

Model number	Model name	Drain current vale (μA/μm)
default	Benchmarking	2500
1	Full ballistic	1137
2	Electrostatic	2182
3	Flux-theory	2548
4	Flux-theory corrected	2548
5	Space charge	2241

Finally, the simulation research work in reference [31] is used as a roadmap prediction for on-state current. This research work focused on 22 nm MOSFET with graphene bilayer channel and the on-state current of 4228 μA/μm has been achieved. Generally, it is clear that Si-based 10 nm DG nano-MOSFETs produce lower on-state drain current than other MOSFET structures with different channel materials. Thus, there is a bright future that researchers all over the world can find new channel materials that can replace or perform better than Si in coming decades.

5. CONCLUSION

Accurate and precise quantum transport models are required by device scientists in order to properly study the behavior of electron flow in ultra-thin and ultra-short nano-MOSFETs by using device simulators. This effort is necessary before the relevant nanodevices can be commercialized in designing electronics circuits and systems. In this paper, a total of five electron transport models for DG nano-MOSFET have been numerically analyzed by referring to norminal on-state drain current value of 2.500×10^3 μA/μm for nano-MOSFET. After performing analysis, it can be concluded that flux-theory based transport models exhibit the best performance efficiency of nearly 100% in term of drain current performance. This is because the electrons behave like wave at quantum limits. This wave nature property cannot be appropriately described with classical drift-diffusion equation. However, the other four models are also acceptable to certain extent. The best practice in developing nanodevice simulators is to incorporate the most efficient carriers transport models in the simulation library.

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